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**TRANSMITTAL LETTER**  
**(General - Patent Pending)**

Docket No.  
51889/3

Application Of: Douglas R. Hackler, Sr. et al.

Serial No.  
10/719,119

Filing Date  
November 21, 2003

Examiner  
Not yet assigned

Group Art Unit  
2814

Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith is:

**Information Disclosure Statement**  
**PTO-1449 with copies of cited articles**  
**Postcard**

in the above identified application.

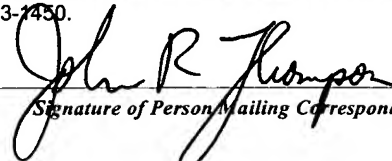
- ☒ No additional fee is required.
- ☐ A check in the amount of \_\_\_\_\_ is attached.
- ☐ The Director is hereby authorized to charge and credit Deposit Account No. \_\_\_\_\_ as described below.
- ☐ Charge the amount of \_\_\_\_\_
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Signature

**John R. Thompson**  
**Registration No. 40,842**  
**STOEL RIVES LLP**  
**One Utah Center**  
**201 South Main Street, Suite 1100**  
**Salt Lake City, UT 84111**  
**Phone: (801) 578-6994; Facsimile: (801) 578-6999**

Dated: March 18, 2004

I certify that this document and fee is being deposited on March 18, 2004 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

  
Signature of Person Mailing Correspondence

**John R. Thompson**

Typed or Printed Name of Person Mailing Correspondence

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

**Douglas R. Hackler, Sr. et al.**

Confirmation No. 1799

Application No. 10/719,119

Filed: November 21, 2003

For: **DOUBLE-GATED TRANSISTOR  
CIRCUIT**

Group Art Unit: 2814

Examiner:

Date: March 18, 2004

INFORMATION DISCLOSURE STATEMENT

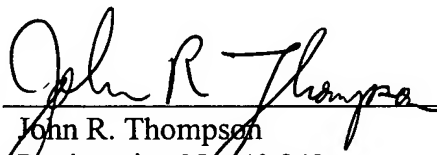
TO THE COMMISSIONER FOR PATENTS:

1. Pursuant to the duty of disclosure, documents listed on the accompanying Form PTO-1449 (or equivalent) are presented for the Examiner's consideration.
  - ☒ Copies of listed documents are enclosed. (37 CFR § 1.98(a))
  - ☒ Copies of listed U.S. patent documents are omitted because this application was filed after June 30, 2003 and is, thus, subject to image file wrapper processing. Copies of listed foreign patent documents and non-patent literature are enclosed.
  - ☐ Copies of the documents listed on sheet(s) \_\_\_\_\_ of Form PTO-1449 (or equivalent) are omitted because (1) they are already of record in U.S. Patent Application No. \_\_\_\_\_, filed \_\_\_\_\_, on which this application relies for an earlier filing date under 35 U.S.C. § 120; and (2) any information disclosure statement filed in the prosecution of Application No. \_\_\_\_\_, complies with 37 CFR §§ 1.98(a) through (c). (37 C.F.R. § 1.98(d))
2. ☐ The Examiner's attention is directed to the enclosed copy of copending U.S. Patent Application No. \_\_\_\_\_, filed \_\_\_\_\_, for \_\_\_\_\_, which is cited in this application.
3. This information disclosure statement is being submitted (check box a., b., or c.):
  - a. ☒ Within three months of the filing date of a national application or entry of the national stage in an international application; or before the mailing of a first Office action on the merits; or before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. (No statement under 37 CFR 1.97(e) is required.); or

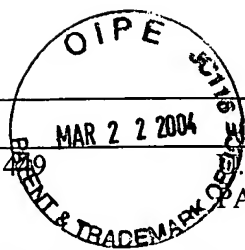


- b. ☐ After the period set forth in paragraph 3a, but before the mailing date of either a final action, a notice of allowance, or an action that otherwise closes prosecution in the application. (Check box i. or ii.)
- i. ☐ A \$180.00 information disclosure statement submission fee set forth in 37 CFR 1.17(p) is enclosed, or
- ii. ☐ A statement specified by 37 CFR 1.97(e) is set forth below; or
- c. ☐ After the mailing date of a final action or notice of allowance and on or before payment of the issue fee. A statement specified by 37 CFR 1.97(e) is set forth below. Enclosed is a \$180.00 information disclosure statement processing fee set forth in 37 CFR 1.17(p).
4. If a statement specified by 37 CFR 1.97(e) is required, the attorney or agent signing below hereby states that:
- ☐ each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; or
- ☐ no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement.
5. ☐ A concise explanation of the relevance of each document not in the English language and/or selected documents in the English language is set forth below.

Respectfully submitted,

By   
John R. Thompson  
Registration No. 40,842

STOEL RIVES LLP  
One Utah Center Suite 1100  
201 S Main Street  
Salt Lake City, UT 84111-4904  
Telephone: (801) 328-3131  
Facsimile: (801) 578-6999  
Attorney Docket No. 51889/3

U.S. DEPARTMENT OF COMMERCE  
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## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	1	2002/0187610 A1	12/12/02	Furukawa et al.	438	283	06/12/01
	2	2002/0153587 A1	10/24/02	Adkisson et al.	257	510	07/02/02
	3	2002/0140039 A1	10/03/02	Adkisson et al.	257	377	06/18/02
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	17	5,349,228	09/20/94	Neudeck et al.	257	365	12/07/93
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	19	3,755,012	08/28/73	George et al.	148	175	03/19/71

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICA- TION DATE	COUNTRY / PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	20							
	21							
	22							
	23							
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## OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication, etc.)

	28	Harada et al., "2-GHz RF Front-End Circuits in CMOS/SIMOX Operating at an Extremely Low Voltage of 0.5 V," IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, December 2000, pgs. 2000-2004.
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52	Tavel et al., "High Performance 40nm nMOSFETs With HfO <sub>2</sub> Gate Dielectric and Polysilicon Damascene Gate," France Telecom R&D, B.P. 98, 38243 Meylan, France, pgs. 17.1.1-17.1.4.
53	Krivokapic et al., "Nickel Silicide Metal Gate FDSOI Devices with Improved Gate Oxide Leakage," AMD, Technology Research Group, M/S 143, One AMD Place, Sunnyvale, CA 94088-3453, USA, pgs. 10.7.1-10.7.4.
54	Monfray et al., "SON (Silicon-On-Nothing) P-MOSFETs with totally silicided (CoSi <sub>2</sub> ) Polysilicon on 5nm-thick Si-films: The simplest way to integration of Metal Gates on thin FD channels," ST Microelectronics, 850, rue J.Monnet, 38921 Crolles, France, pgs. 10.5.1-10.5.4.
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57	Wong et al., "Device Design Considerations for Double-Gate, Ground-Plane, and Single-Gated Ultra-Thin SOI MOSFET's at the 25 nm Channel Length Generation," IBM T.J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598, U.S.A., pgs. 15.2.1-15.2.4.
58	Guarini et al., "Triple-Self-Aligned, Planar Double-Gate MOSFETs: Devices and Circuits," IBM T.J. Watson Research Center, Yorktown Heights, New York 10598, U.S.A., pgs. 19.2.1-19.2.4.
59	Solomon et al., "Two Gates Are Better Than One," IEEE Circuits & Devices Magazine, January 2003, pgs. 48-63.
60	Cheng et al., "The Impact of High- $\kappa$ Gate Dielectrics and Metal Gate Electrodes on Sub-100 nm MOSFET's," IEEE Transactions on Electron Devices, Vol. 46, No. 7, July 1999, pgs. 1537-1544.

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65	Yagishita et al., "Dynamic Threshold Voltage Damascene Metal Gate MOSFET (DT-DMG-MOS) with Low Threshold Voltage, High Drive Current, and Uniform Electrical Characteristics," Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan, pgs. 29.2.1-29.2.4.
66	Samavedam et al., "Dual-Metal Gate CMOS with HfO <sub>2</sub> Gate Dielectric," Motorola Digital DNA™ Laboratories, 3501 Ed Bluestein Blvd., MD:K10, (*AMD), Austin, TX 78721, USA, pgs. 17.2.1-17.2.4.
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83	Choi et al., "FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering," Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA, pgs. 10.4.1-10.4.4.
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